UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,403	01/09/2004	Takumi Yamaguchi	10873.1377US01	7971

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HAMRE, SCHUMANN, MUELLER & LARSON P.C.
P.O. BOX 2902-0902
MINNEAPOLIS, MN 55402

EXAMINER
PETERSON, CHRISTOPHER K

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/754,403	YAMAGUCHI ET AL.
	Examiner	Art Unit	
	CHRISTOPHER K. PETERSON	2622	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2008*.

2a)☐ This action is **FINAL**.　　　2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☒ All　b)☐ Some * c)☐ None of:

　　　1.☒ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on

4/14/2008 has been entered.

Response to Arguments

2.   Applicant's arguments filed 4/14/2008 have been fully considered but they are

not persuasive.

        First in regard to claims 1 and 2, the Applicant has amended the claims to

include the limitation "output of the adding circuit is subjected to a gain control directly

by the gain control portion and then stored in the storage portion". The Applicant

argues that Voss cannot teach or suggest that a gain of the adding circuit is controlled

directly by a gain control portion within the adding circuit as required by claims 1 and 2.

The Examiner Respectfully disagrees. Specifically, noting Fig. 1 and Col. 6, lines 50 –

67 shows the CMOS sensor (24) is directly controlled by the variable analog amplifier

(26). Voss teaches that the CMOS sensor (24) is where the summing (adding) process

takes place. Voss also teaches that the light level sensor (55) provides a signal to the

microprocessor (32), which then provides the gain signal to the variable analog amplifier

(26) and a CMOS resolution signal to the CMOS sensor (24). The applicant's

specification teaches that a gain control circuit (11) generates the control gain control

signal based on an output signal of the photometer portion (12) (Applicant's Spec. Pg 5,

lines 34 – 37). For this reason, the Examiner believes that Voss in view of Fossum do

teach the adding portion (CMOS sensor 24) of the adding circuit is subjected to a gain

control (output of D/A 30) directly by the gain control portion (variable analog amplifier

26) and then stored in the storage portion (memory card 38) (Col. 5, lines 7 – 17 and

Col. 5, line 54 – Col. 6, line 4) and the rejection to the claim will be set forth below.

Claim Rejections - 35 USC § 103

3.   The text of those sections of Title 35, U.S. Code not included in this action can

be found in a prior Office action.

4.   **Claims 1 – 5 and 8 - 20 are rejected under 35 U.S.C. 103(a) as being**

unpatentable over Voss (US Patent # 7,233,354) in view of Fossum (US Patent #

5,949,483).

As to claim 1, Voss teaches a solid-state imaging device, comprising:

- an imaging region (CMOS sensor 24) in which a plurality of pixels are

  arranged (Col. 4, lines 41 – 44); and

- wherein an adding circuit (CMOS sensor 24, variable analog amplifier 26,

  A/D converter 28, microprocessor 32 and memory card 38) for adding pixel

  signals obtained from two or more of the pixels is provided so that an output

signal of the adding circuit is read out to the signal line (Col. 6, line 53 – 59),
the adding circuit comprising an adding portion (summed pixels Col.6, lines
57 - 59), a gain control portion (variable analog amplifier 26) and a storage
portion (memory card 38), so that an output of the adding circuit (24) is
subjected to a gain control directly by the gain control portion (26) and then
stored in the storage portion(38) (Col. 4, lines 61 – 65), and

- wherein on the basis of a predetermined reference quantity of light (light-
  level sensor 55) incident onto the imaging region (24), a gain of the adding
  circuit in a condition in which a quantity of the incident light is above the
  reference quantity is controlled to be smaller than a gain of the adding circuit
  in a condition in which a quantity of the incident light is below the reference
  quantity (Col. 5 line 54 – Col.6, line 4). Voss teaches the microprocessor
  decides to adjust the gain, resolution, or both depending on the light-level
  sensor (55). The microprocessor would provide a small gain when in the
  incident light is high and provide a large gain for low incident light (Col. 5 line
  62 – Col.6, line 4).

Voss does not teach a signal line through which a pixel signal of the imaging
region is read out. Fossum (Fig. 8) teaches a signal line (output signals from
multiplexer 612) through which a pixel signal of the imaging region is read out (Col. 11,
lines 34 – 40). Therefore, it would have been obvious to one of ordinary skill in the art
at the time the invention was made to have provided signal line through which a pixel
signal of the imaging region is read out as taught by Fossum to the imaging device of

Voss, because a multi-resolution readout system that can provide image data at a
desired resolution and at speeds greater than or equal to the aforementioned video
rates Col. 2, lines47 – 50 of Fossum)

　　　As to claim 2, Voss teaches a solid-state imaging device, comprising:

- an imaging region (CMOS sensor 24) in which a plurality of pixels are
  arranged (Col. 4, lines 41 – 44); and

- wherein an adding circuit (CMOS sensor 24, variable analog amplifier 26,
  A/D converter 28, microprocessor 32 and memory card 38) for adding pixel
  signals obtained from two or more of the pixels is provided so that an output
  signal of the adding circuit is read out to the signal line (Col. 6, line 53 – 59),
  the adding circuit comprising an adding portion (summed pixels Col.6, lines
  57 - 59), a gain control portion (variable analog amplifier 26) and a storage
  portion (memory card 38), so that an output of the adding circuit (24) is
  subjected to a gain control directly by the gain control portion (26) and then
  stored in the storage portion(38) (Col. 4, lines 61 – 65), and

- wherein within at least a partial range of a quantity of incident light onto the
  imaging region (24), a gain of the adding circuit is controlled to decrease
  with an increase of the quantity of the incident light (Col. 5 line 54 – Col.6,
  line 4). Voss teaches the microprocessor decides to adjust the gain,
  resolution, or both depending on the light-level sensor (55). The
  microprocessor would provide a small gain when in the incident light is high
  and provide a large gain for low incident light (Col. 5 line 62 – Col.6, line 4).

Voss does not teach a signal line through which a pixel signal of the imaging region is read out. Fossum (Fig. 8) teaches a signal line (output signals from multiplexer 612) through which a pixel signal of the imaging region is read out (Col. 11, lines 34 – 40). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided signal line through which a pixel signal of the imaging region is read out as taught by Fossum to the imaging device of Voss, because a multi-resolution readout system that can provide image data at a desired resolution and at speeds greater than or equal to the aforementioned video rates Col. 2, lines47 – 50 of Fossum)

As to claim 3, Voss in view of Fossum teaches wherein the adding circuit (24, 26, 28, 32 and 38 of Voss) is arranged between the imaging region (image array 602 of Fossum) and the signal line (output signals from multiplexer 612 of Fossum).

As to claim 4, Voss teaches the solid-state imaging device according to claim 1,wherein a plurality of the adding circuits are arranged between the two or more pixels included in the respective sets of pixels (Col. 6, lines 50 – 53).

As to claim 5, Voss teaches the solid-state imaging device according to claim 1,wherein a plurality of the adding circuits are provided, and gains for at least two of the plurality of adding circuits are controlled individually (Col.6., line 50 – 67). Voss teaches the summing function occurs before any gain is applied to the signal (Col. 6, line 59 – 64). This increases the signal to noise ratio.

As to claim 8, note the discussion above. Voss does not teach an adding circuit is provided with an averaging portion. Fossum (Fig. 7 and 8) teaches an averaging

portion (608 and 610) for averaging pixel signals obtained from two or more of the
pixels(Col. 11, lines 3 – 40). Fossum (Fig. 8) shows how a block of 3 x 3 would be
processed through the averaging circuit (608 and 610) (Col. 11, lines 23 – 32). Fossum
also teaches the multi-resolution readout architecture can be set by programmable
switches (Col. 12, lines 14 - 20). The microprocessor of Voss and the programmable
switches of Fossum could be the same unit. When the quantity of incident light is larger
than a predetermined higher reference quantity that is larger, than the reference
quantity, an output of the averaging portion is read out to the signal line in place of the
added signal (Col. 11, lines 3 – 40). Fossum (Fig. 8) shows how a block of 3 x 3 would
be processed through the averaging circuit (608 and 610) (Col. 11, lines 23 – 32).

As to claim 9, Voss teaches wherein when signals of N pieces of pixels (added
pixels) are added, a gain of the adding circuit (24, 26, 28, 32 and 38) is controlled so
that an output value from the adding circuit is not more than a value obtained from the
following formula: (value obtained by adding the N pieces of signals) / N (Col. 5 line 62
– Col.6, line 4). Voss teaches the microprocessor decides to adjust the gain, resolution,
or both depending on the light-level sensor (55). The microprocessor would provide a
small gain when in the incident light is high and provide a large gain for low incident light
(Col. 5 line 62 – Col.6, line 4).

As to claim 10, Voss teaches wherein when signals of N pieces of pixels are
added, a gain of the adding circuit (24, 26, 28, 32 and 38) is controlled so that an output
value from the adding circuit is less than a value obtained by adding the N pieces of
signals and more than a value obtained from the following formula: (value obtained by

adding the N pieces of signals) / N (Col. 5 line 62 – Col.6, line 4). Voss teaches the

microprocessor decides to adjust the gain, resolution, or both depending on the light-

level sensor (55). The microprocessor would provide a small gain when in the incident

light is high and provide a large gain for low incident light (Col. 5 line 62 – Col.6, line 4).

As to claim 11, Voss teaches a camera (10) equipped with the solid-state

imaging device according to claim 1 (Col. 3, lines 42 – 51).

As to claim 19, Voss teaches wherein a gain (26) is controlled for each of the

plurality of signals (Col. 5, line 54 – Col. 6, line 4). Voss teaches the microprocessor

(32) decides if the gain is used or change in resolution.

As to claims 12 – 18 and 20, these claims differ from claims 1, 3, 4, 5 – 11 and

19 only in that the claims 12 – 18 and 20 depend on claim 2 and claims 1, 3, 4, 5 – 11

and 19 depend on claim 1. Thus claims 12 – 18 and 20 are analyzed as previously

discussed with respect to claims 1, 3, 4, 5 – 11 and 19 above.

5.   **Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable
over Voss (US Patent # 7,233,354) in view of Fossum (US Patent # 5,949,483) as
applied to claims 3 and 4 above, and further in view of Takayama (US Patent #
7,088,395).**

As to claim 6, note the discussion of Voss in view of Fossum above, Voss in view

of Fossum do not teach a photometer portion is provided between the imaging region

and the signal line so as to detect a quantity of the incident light onto the imaging

region. Takayama teaches a photometer portion (150b) is provided between the

imaging region (54) and the signal line (w1 and w2) so as to detect a quantity of the

incident light onto the imaging region (54). Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to have provided a

photometer portion is provided between the imaging region and the signal line so as to

detect a quantity of the incident light onto the imaging region as taught by Takayama to

the image capturing device of Voss in view of Fossum, because the image-capturing

apparatus will reduce its power consumption, low-cost and reduce the number of

necessary parts (Col. 2, line 62 – Col. 3, line 10 of Takayama).

As to claim 7, claim 7 cites a photometer portion is arranged between the two or

more pixels as to claim 6. Takayama teaches a photometer portion (50b in Fig. 4) is

arranged between the two or more pixels (50a).

6.   **Claims 21 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable**

over Voss (US Patent # 7,233,354) in view of Fossum (US Patent # 5,949,483) as

applied to claims 1 and 2 above, and further in view of Sharma (US Patent Pub. #

2004/0008542).

As to claim 21, Voss in view of Fossum teach a storage portion. Voss in view of

Fossum do not specifically teach a storage portion composed of a capacitor. Sharma

teaches a memory backup system. The memory back-up system includes a first

memory cell, and a non-volatile memory cell that is interfaced to the first memory cell.

Control circuitry allows data to be written to either the first memory cell or the non-

volatile memory cell, and provides transfer of the data from either the first memory cell

or the non-volatile memory cell, to the other of either the first memory cell or the non-volatile memory cell. Sharma (Fig. 3) teaches the storage portion (DRAM / MRAM memory cell 300) is composed of a capacitor (CD) (Para 28 and 29). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a DRAM / MRAM memory cell as taught by Sharma to the image capturing device of Voss in view of Fossum, because the memory system allows for efficient transfer of large amounts of data between the volatile and non-volatile memory (Para 14 of Sharma).

As to claim 22, this claim differs from claim 21 only in that the claim 22 depends on claim 2 whereas claim 21 depends on claim 1. Thus method claim 22 is analyzed as previously discussed with respect to claim 21 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER K. PETERSON whose telephone number is (571)270-1704. The examiner can normally be reached on Monday - Friday 6:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CKP
23 May 2008

/Timothy J Henn/
Primary Examiner, Art Unit 2622